A HW/SW Unified Approach for Embedded System Monitoring

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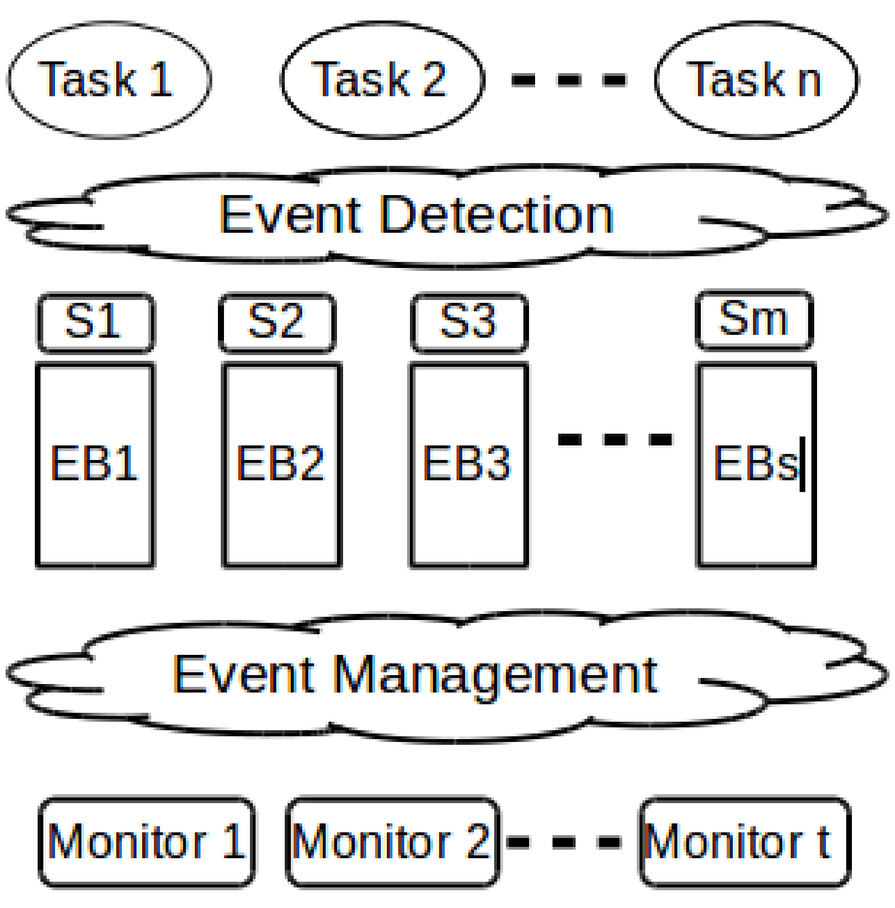
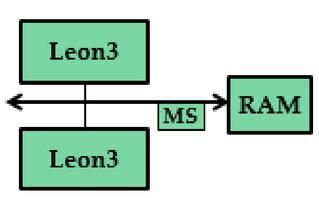
Motivations – Proposed Solution

- **Embedded systems are characterized, in general, by multiple constraints and limited resources. Dealing with such conflicting issues can drive to complex heterogeneous platforms. Different phases of the product lifecycle can be identified:**
  - **<u>DESIGN TIME</u>: during the development phases, a mapping of tasks onto software and hardware components, namely a *Design Space Exploration*, is required. A *Monitoring Solution* can offer a profile of the behaviour of the application/platform components, in order to support the designer on this mapping action. This is Profiling.**
  - ***RUNTIME*: during the Runtime of the application on the final platform, different actions can be executed on it in order to verify if the system is working as expected. A *Monitoring Solution* can offer support for:**
    - **Runtime Validation: it offers the "probes" (SW or HW) that serve to validate the satisfaction of functional requirements**
    - **Runtime Verification: it offers the elements necessary to verify that a non-functional property is satisfied.**
    - **Providing feedback to the model in order to refine it**
- **In this context, this work proposes a generalization of the concept of monitoring by defining a general reference architecture that can be adapted to different applications.**

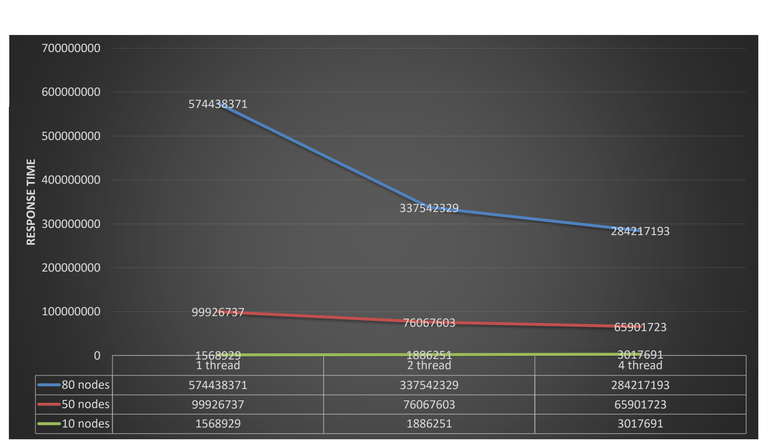
Generalization of Monitoring Infrastructure



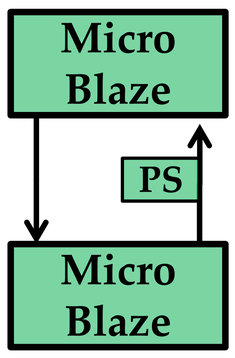
Profiling of OpenMP applications



- **Response Time measure**

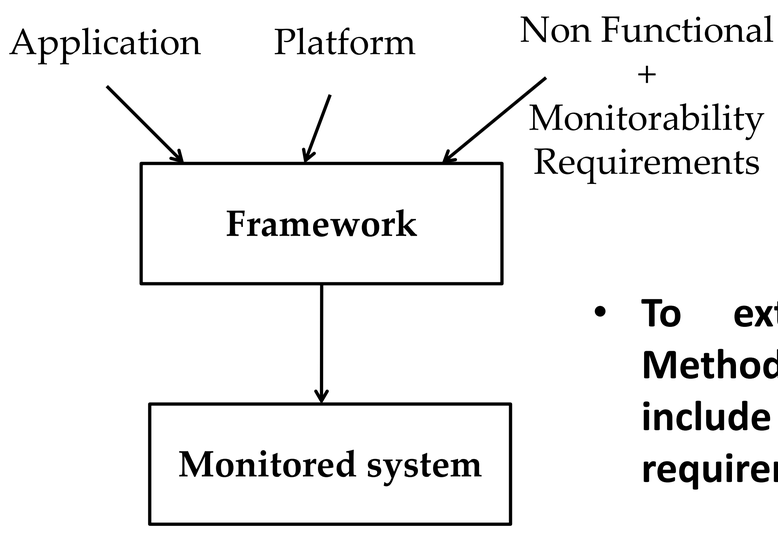


Runtime Verification



Stalls identification in multi-MicroBlaze system scenario

Future Steps



- **To extend Hepsycode Methodology in order to include "Monitorability requirements"**

References

[1] G. Valente, "A framework for integrated monitoring of real-time embedded SoC," 2015 25th International Conference on Field Programmable Logic and Applications (FPL), London, 2015, pp. 1-2

[2] A. Moro, F. Federici, G. Valente, L. Pomante, M. Faccio and V. Muttillo, "Hardware performance sniffers for embedded systems profiling," 2015 12th International Workshop on Intelligent Solutions in Embedded Systems (WISES), Ancona, 2015, pp. 29-34.

[3] G. Valente, V. Muttillo, L. Pomante, F. Federici, M. Faccio, A. Moro, C. Tieri, S. Ferri "A Flexible Profiling Sub-System for Reconfigurable Logic Architectures," 2016 24th Euromicro International Conference on Parallel, Distributed, and Network-Based Processing (PDP), Heraklion, 2016, pp. 373-376.

[4] V. Muttillo, G. Valente, F. Federici, L. Pomante, M. Faccio, C. Tieri, S. Ferri "A design methodology for soft-core platforms on FPGA with SMP Linux, OpenMP support, and distributed hardware profiling system", EURASIP Journal on Embedded Systems 2016: 15. doi:10.1186/s13639-016-0051-9

[5] M. Faccio, F. Federici, G. Marini, V. Muttillo, L. Pomante and G. Valente, "Design and validation of multi-core embedded systems under time-to-prototype and high performance constraints," 2016 IEEE 2nd International Forum on Research and Technologies for Society and Industry Leveraging a better tomorrow (RTSI), Bologna, 2016, pp.1-1.